

ABSTRACT

[0047] A pixel circuit, and a method for operating a high-low sensitivity (HLS) pixel circuit, to provide increased dynamic range in an imager. The pixel circuit combines a four transistor ("4T") and a three-transistor plus capacitor ("3TC") configuration in one pixel, where the 4T portion of the pixel is coupled to a high sensitivity buried photodiode region, and the 3TC portion of the pixel is coupled to a low sensitivity buried photodiode region. The pixel circuit first reads out charge from the high sensitivity photodiode region and compares it to a reset voltage, then reads out charge from the low sensitivity photodiode region. Under an alternate embodiment, multiple HLS pixels are coupled through a common floating diffusion node.